AMENDMENT TO THE SPECIFICATION

Please amend the specification as follows:

At page 6, the paragraph commencing at line 6.

Fig. 8~~s~~ is a graph illustrating an improvement in the reception accuracy achieved in accordance with the present invention.

At page 9, the paragraph commencing at line 6.

Fig. 5 shows a filter configuration for performing the second phase of initial signal acquisition. As previously stated, an objective of this second phase is to recover the secondary synchronization code from the received signal. Recovery of this code is accomplished using two stages of matched filters, which may also be characterized as Stage 1 filter 501 and Stage 2 filters 502, and a magnitude determination circuit 510. The Stage 1 filter 501 searches for sequence *b* in the received secondary synchronization sub-channel, which sequence may be represented as:

At page 14, the paragraph commencing at line 7.

As previously stated, the outputs from the magnitude determination circuits are summed (non-coherently combined) in the summation circuit~~770~~ 719. The resulting sequence from circuit~~770~~ 719 spans the 15 time slots illustratively shown in Fig. 2 and identifies a code group which may be mapped to the secondary synchronization code (SSC) in accordance with the following definition:

At page 15, the paragraph commencing at line 19.

More specifically, a frequency offset of 10 kHz shows only about 1 dB of degradation compared to no frequency offset. It is also seen that the second phase impairs performance only about 1 dB beyond the first phase, proving that catastrophic ambiguity is resolved and the matched filter of the present invention provides high performance for phase II acquisition for W-CDMA with robustness to frequency offset errors up to 10 kHz or 5 PPM for 2 ~~Ghz~~ GHz operating frequencies.